DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

VLSI DESIGN LAB MANUAL

PVP20 REGULATIONS

III B.TECH II SEM

PRASAD V POTLURI SIDDHARTHA INSTITUTE OF TECHNOLOGY
(Autonomous, Accredited by NBA & NAAC, an ISO 9001:2015 certified institution)
(Sponsored by Siddhartha Academy of General & Technical Education)
VIJAYAWADA – 520 007

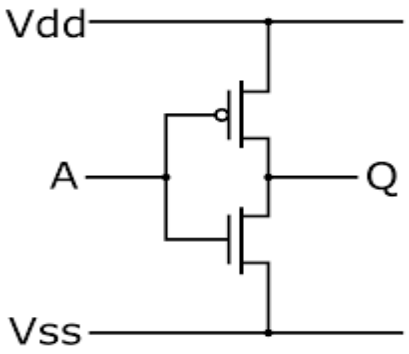
EXPERIMENT 1

CMOS Inverter

AIM: To Design and simulate CMOS Inverter using VLSI CAD tools.

APPARATUS: PC loaded with VLSI CAD tools

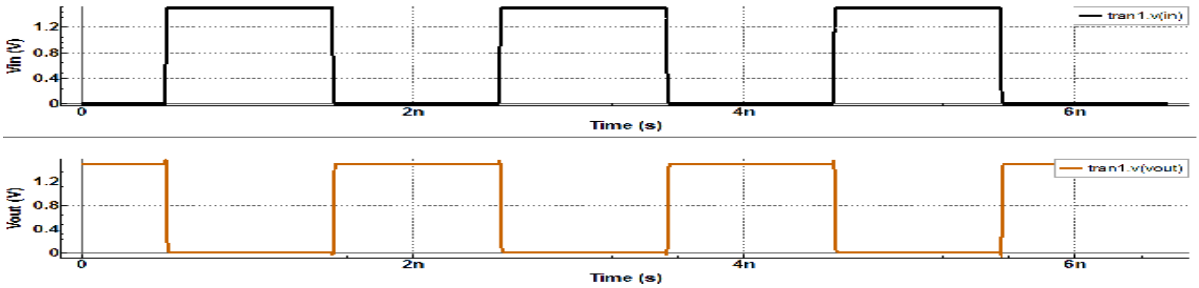
Schematic:



Input	Output
1	0
0	1

Truth table

Model waveform:



Procedure:

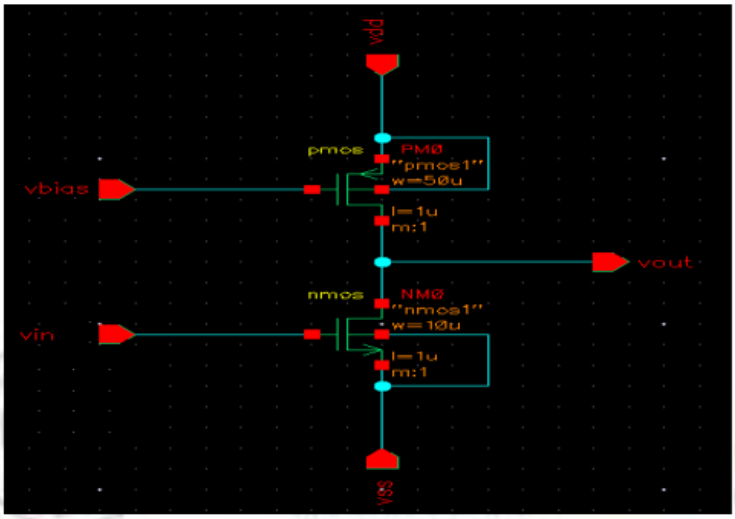
1. Open the VLSI CAD tool software.
2. Construct the circuit
3. Observe the output waveforms VLSI CAD tool software

Result:

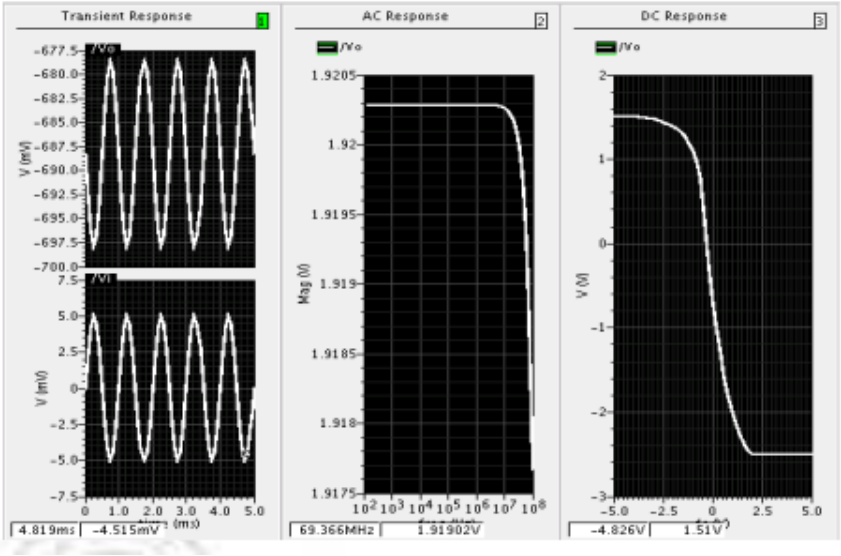
EXPERIMENT 2

COMMON SOURCE AMPLIFIER

Schematic



Model wave form



Procedure:

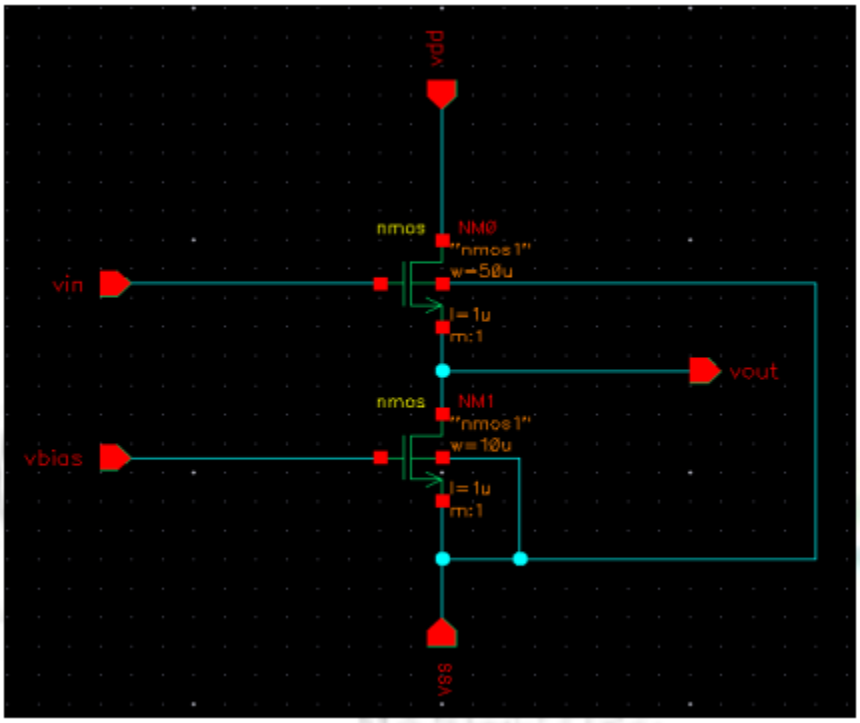
1. **Open the VLSI CAD tool software.**
2. **Construct the circuit**
3. **Observe the output waveforms VLSI CAD tool software**

Result:

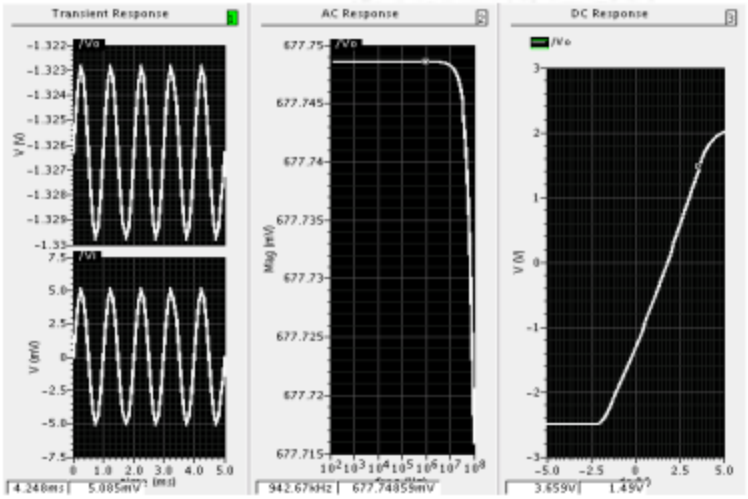
EXPERIMENT 3

COMMON DRAIN AMPLIFIER

Schematic Capture



Model wave form



Procedure:

1. **Open the VLSI CAD tool software.**
2. **Construct the circuit**
3. **Observe the output waveforms VLSI CAD tool software**

Result:

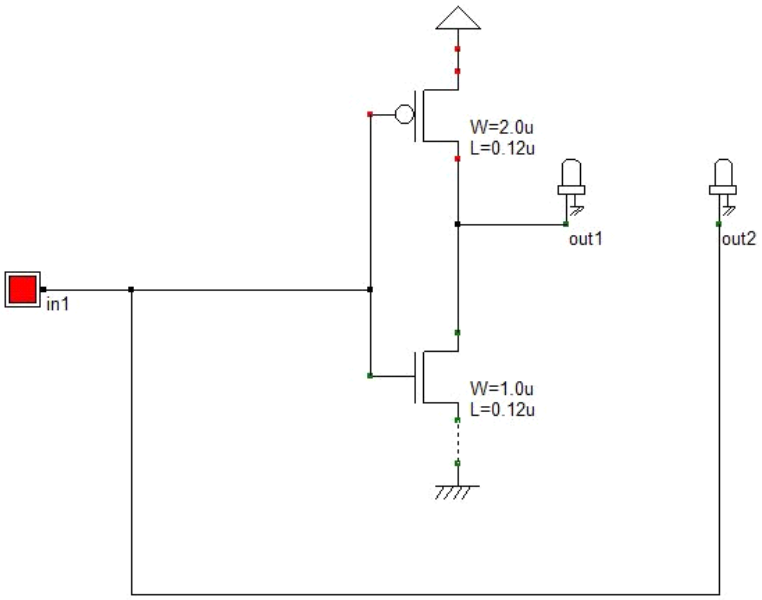
EXPERIMENT 4

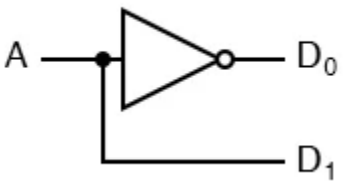
DECODER

AIM: To Design and simulate decoder using VLSI CAD tools.

APPARATUS: PC loaded with VLSI CAD tools

Schematic:

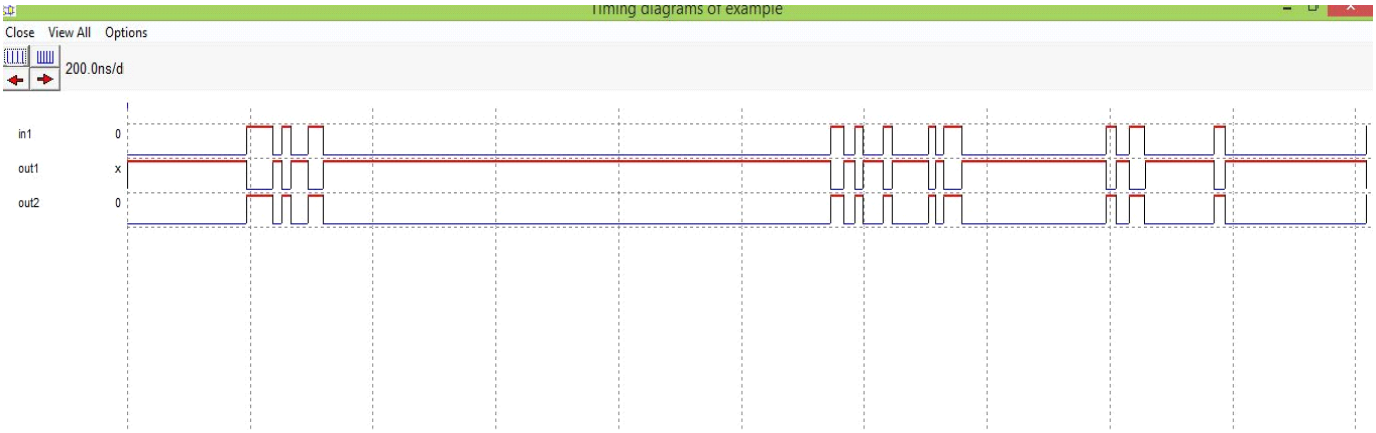




Truth table:

A	D_1	D_0
0	0	1
1	1	0

Model Wave forms:



Procedure:

4. Open the VLSI CAD tool software.
5. Construct the circuit
6. Observe the output waveforms VLSI CAD tool software

Result:

EXPERIMENT 5

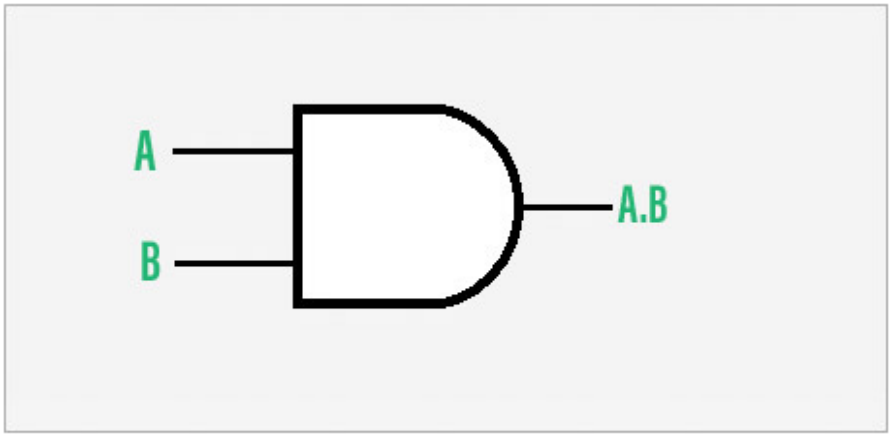
Basic GATES

AIM: To Design and simulate gates using VLSI CAD tools.

APPARATUS: PC loaded with VLSI CAD tools

Schematic:

AND gate:

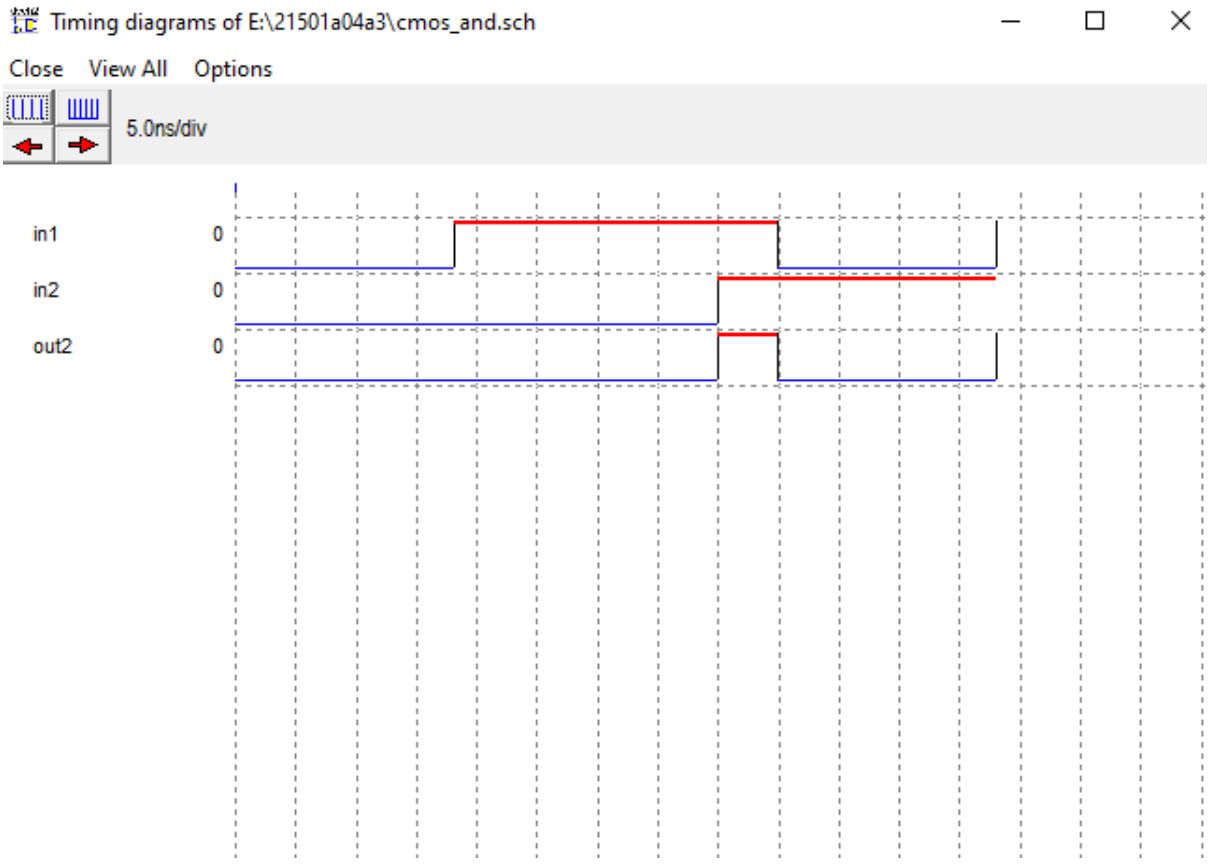


Symbol of Two-Input AND Gate

Truth table:

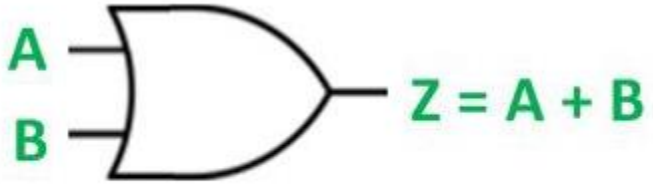
Input		Output
A	B	A AND B
0	0	0
0	1	0
1	0	0
1	1	1

Model waveforms



OR gate:

Schematic:

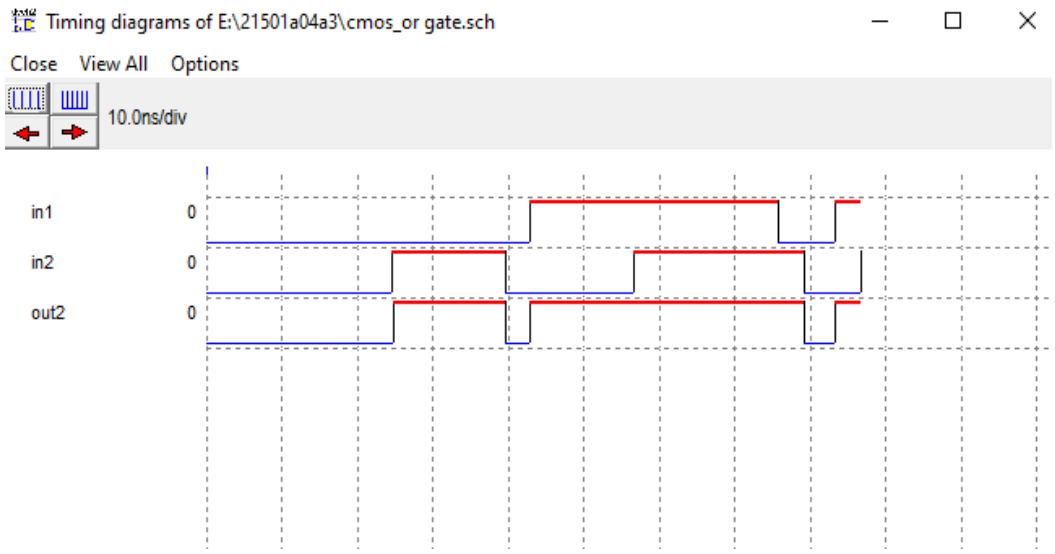


Symbol of Two-Input OR Gate

Truth table:

Input		Output
A	B	A OR B
0	0	0
0	1	1
1	0	1
1	1	1

Model Wave forms:



Procedure:

1. Open the VLSI CAD tool software.
2. Construct the circuit
3. Observe the output waveforms VLSI CAD tool software

Result:

EXPERIMENT 6

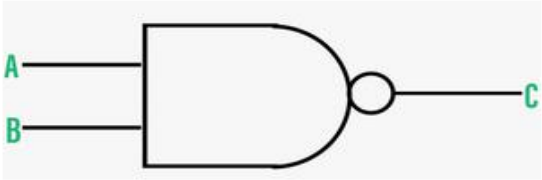
Universal GATEs

AIM: To Design and simulate universal gates using VLSI CAD tools.

APPARATUS: PC loaded with VLSI CAD tools

NAND gate:

Schematic

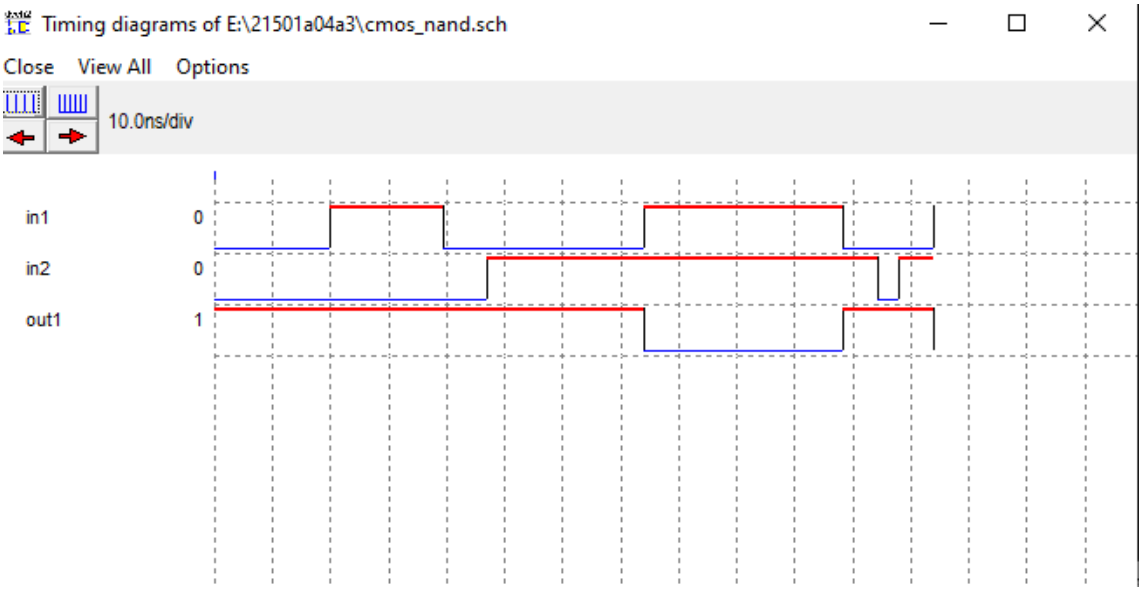


Symbol of NAND Gate

Truth table:

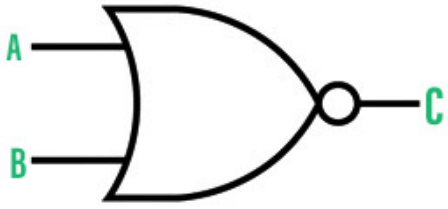
Input		Output
A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

Model wave forms:



NOR gate:

Schematic:

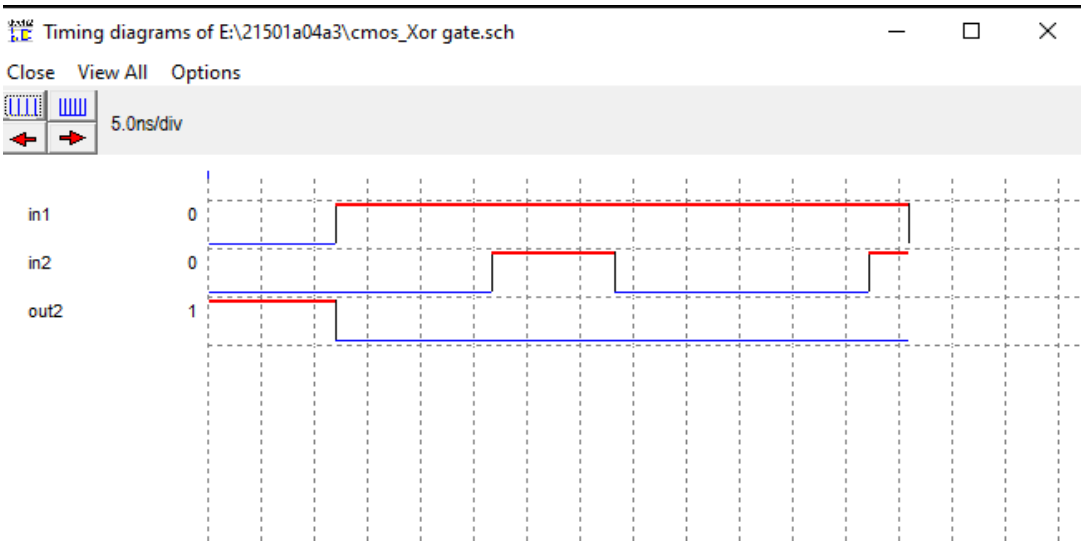


Symbol of the NOR Gate

Truth table:

A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

Model Wave forms:



Procedure:

1. Open the VLSI CAD tool software.
2. Construct the circuit
3. Observe the output waveforms VLSI CAD tool software

Result:

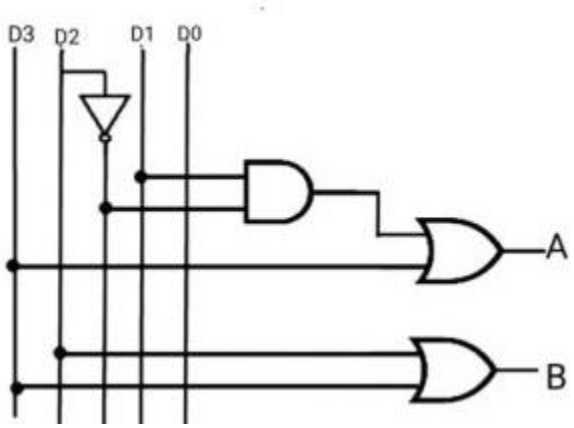
EXPERIMENT 7

PRIORITY ENCODER

AIM: To Design and simulate Priority Encoder using VLSI CAD tools.

APPARATUS: PC loaded with VLSI CAD tools

Schematic:



Logic Equations:

$$A = D3 + D1D2'$$

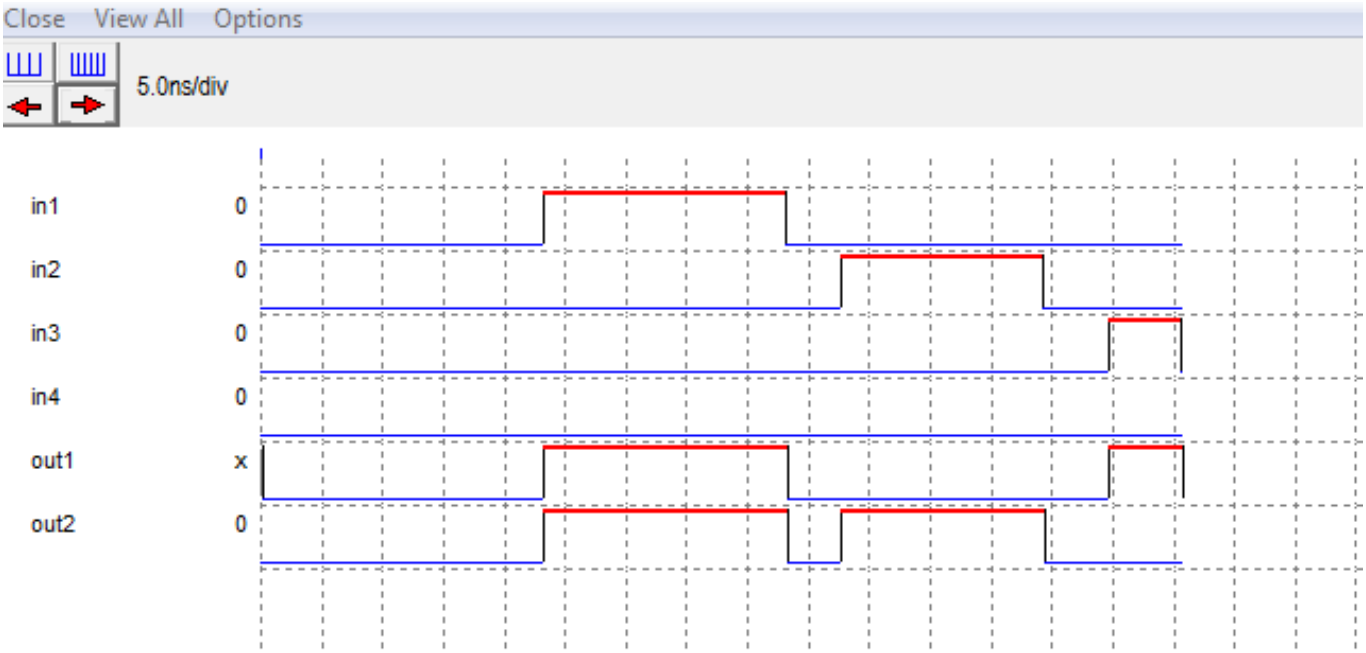
$$B = D2 + D3$$

$$V = D0 + D1 + D2 + D3$$

Truth table:

D3	D2	D1	D0	A	B	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

Model Wave forms:



Procedure:

1. Open the VLSI CAD tool software.
2. Construct the circuit
3. Observe the output waveforms VLSI CAD tool software

Result:

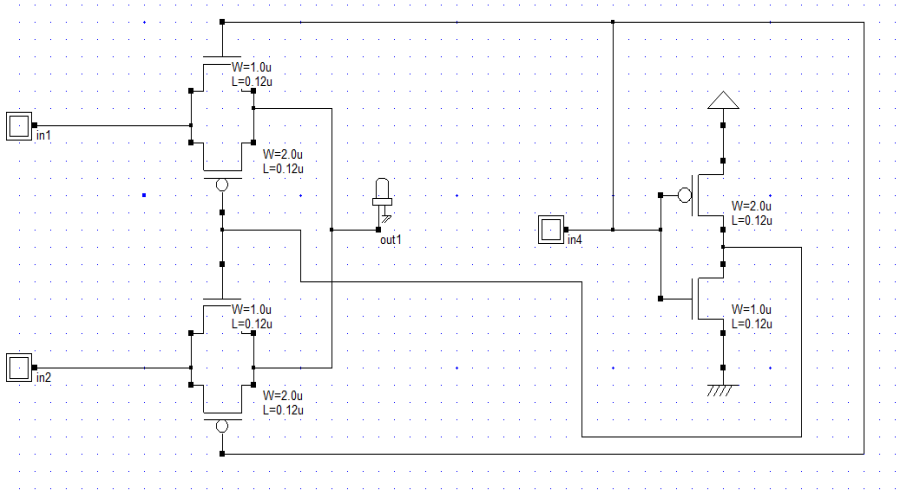
EXPERIMENT 8

MULTIPLEXER

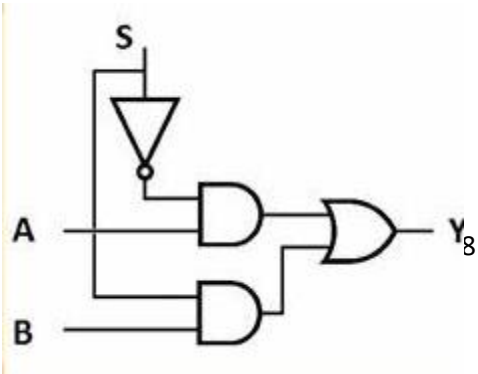
AIM: To Design and simulate multiplexer using VLSI CAD tools.

APPARATUS: PC loaded with VLSI CAD tools

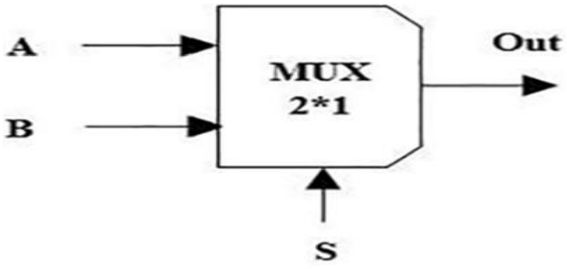
Schematic:



Logicdiagram



Truth Table:



(a)

S	Out
0	B
1	A

(b)

A	B	S	Out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(c)

Procedure:

4. Open the VLSI CAD tool software.
5. Construct the circuit
6. Observe the output waveforms VLSI CAD tool software

Result:

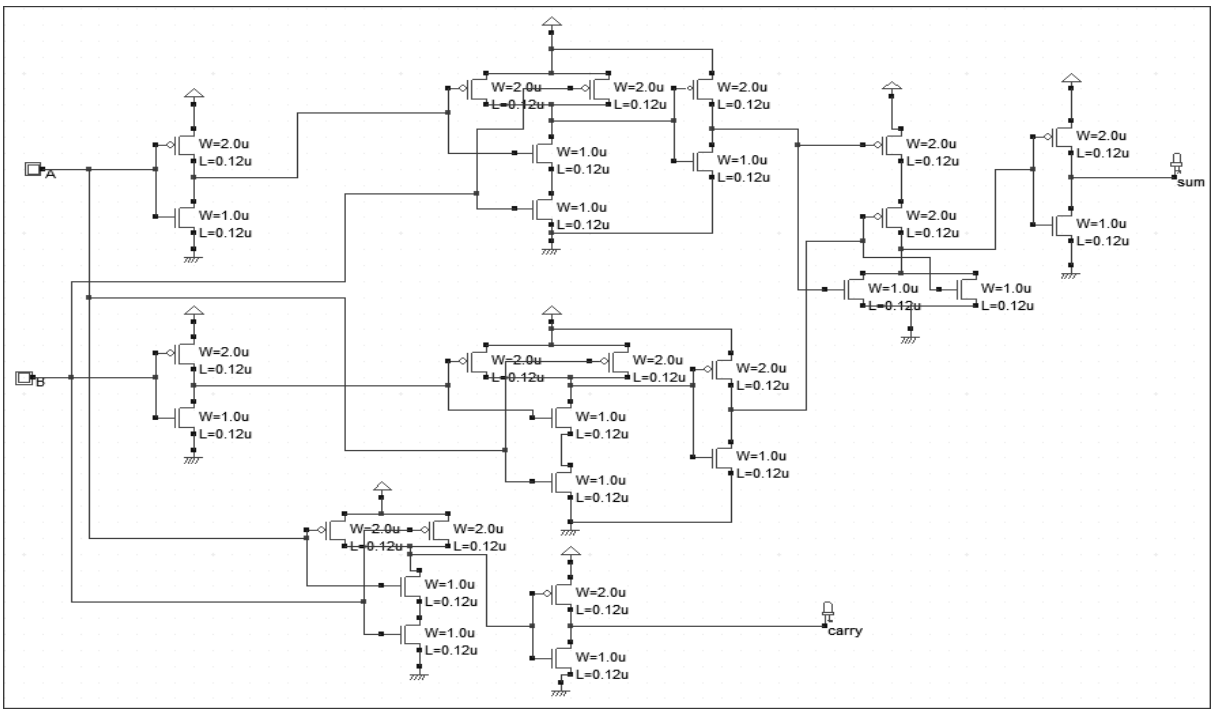
EXPERIMENT 9

HALF ADDER

AIM: To Design and simulate Half Adder using VLSI CAD tools.

APPARATUS: PC loaded with VLSI CAD tools

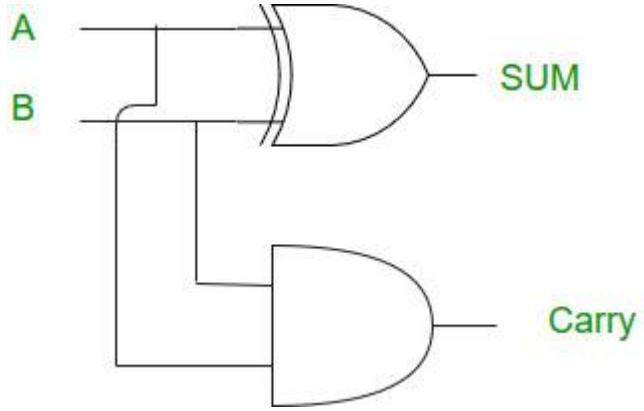
Schematic:



Truth table:

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

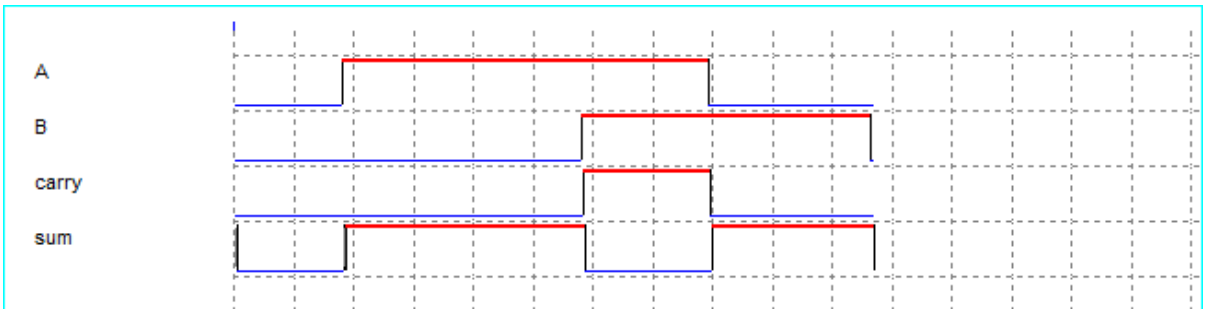
Logic Diagram:



Sum = A XOR B

Carry = A AND B

Model Waveforms:



Procedure:

1. Open the VLSI CAD tool software.
2. Construct the circuit
3. Observe the output waveforms VLSI CAD tool software

Result:

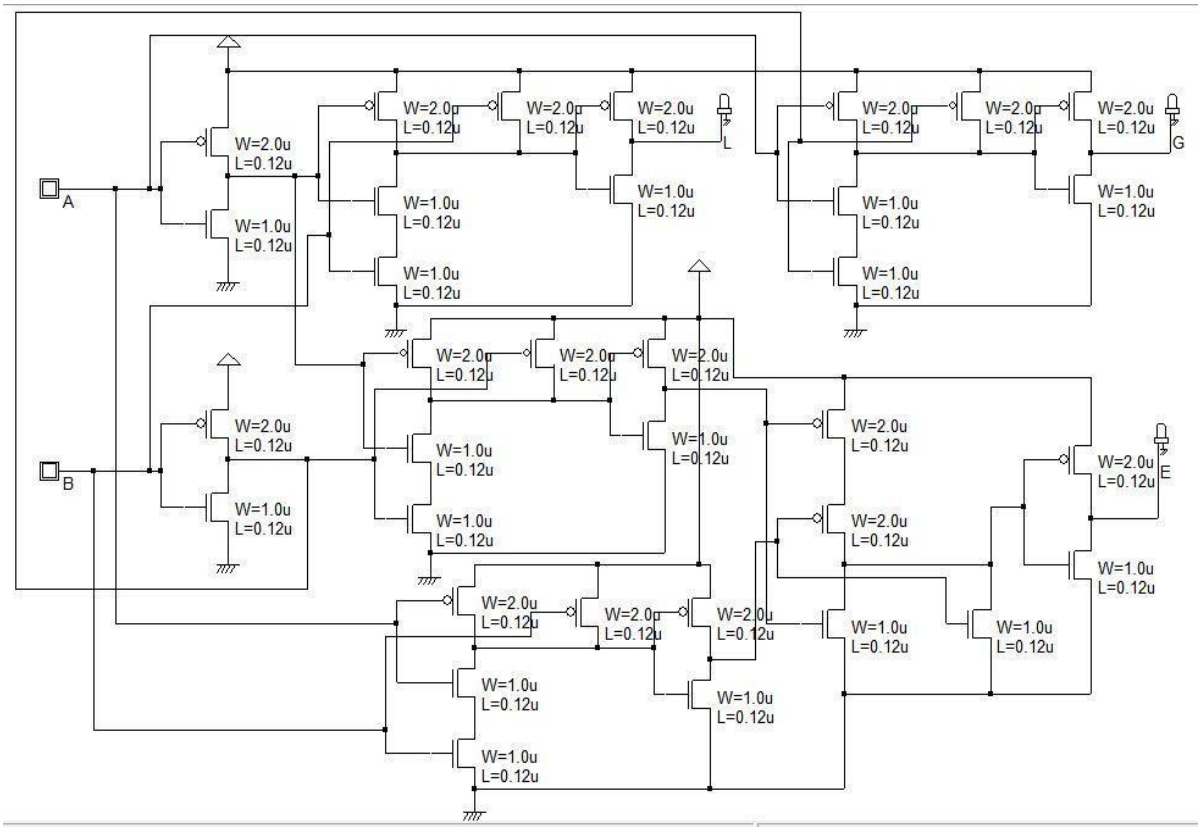
EXPERIMENT 10

COMPARATOR

AIM: To Design and simulate Comparator VLSI CAD tools.

APPARATUS: PC loaded with VLSI CAD tools

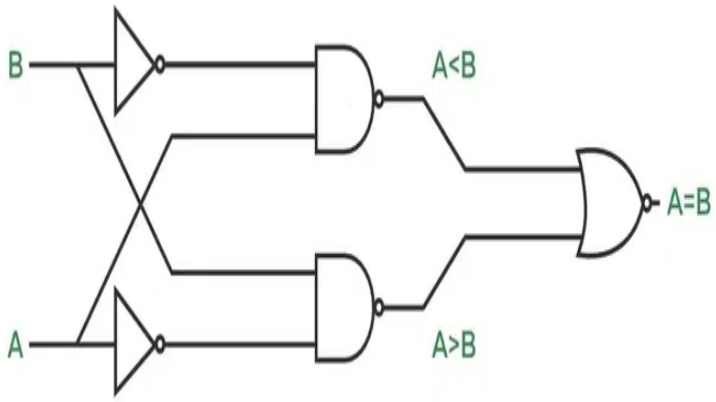
Schematic:



Truth table:

A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

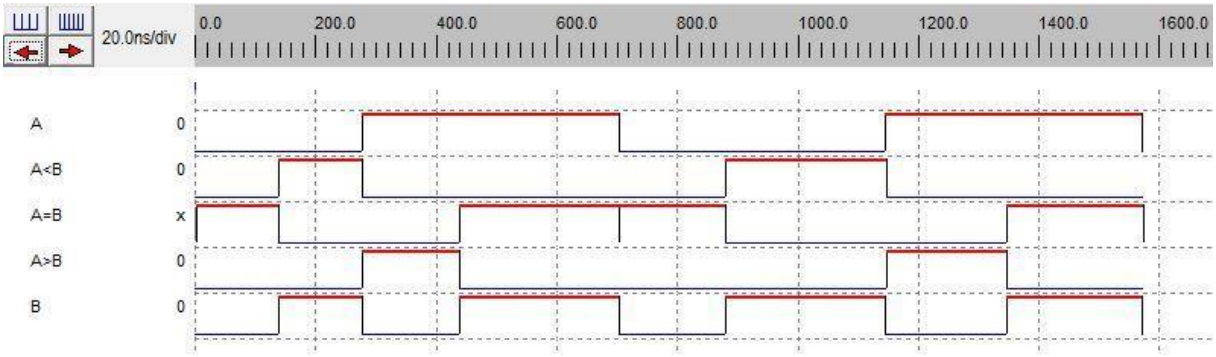
Logic diagram:



equations

A>B= AB'
A<B= A'B
A=B:A'B' + AB

Model Waveforms:



Procedure:

1. Open the VLSI CAD tool software.
2. Construct the circuit
3. Observe the output waveforms VLSI CAD tool software

Result: